Amendments to Claims:

The following listing of claims replaces all previous versions and listings of claims in the application:

1. (Currently amended) A liquid crystal display apparatus, comprising:

a timing controller to generate a plurality of compensated grayscale data;

a memory to store at least grayscale data ~~or the compensated grayscale data~~;

a column driver to apply the compensated grayscale data to a plurality of data lines;

a gate driver to apply a gate signal to a plurality of gate lines; and

a liquid crystal panel including the gate lines, the data lines and a plurality of switching elements disposed between the data lines and the gate lines;

wherein the timing controller comprises:

a data compensator to generate current frame first compensated grayscale data in response to receiving previous frame grayscale data from the memory and current frame grayscale data from an external source;

a difference calculator to calculate a data difference between the current frame first compensated grayscale data and the current frame grayscale data, the difference calculator receiving the current frame first compensated grayscale data from the data compensator; and

a grayscale modifier to generate current frame second compensated grayscale data in response to receiving the current frame first compensated grayscale data from the data compensator and the data difference of the previous frame compensated grayscale data and the previous frame grayscale data from the frame memory.

2. (Cancelled).

3. (Currently amended) A~~The~~ liquid crystal display apparatus ~~according to claim 1, wherein the timing controller~~ comprising:

a timing controller to generate a plurality of compensated grayscale data;

a memory to store at least grayscale data;

a column driver to apply the compensated grayscale data to a plurality of data lines;

a gate driver to apply a gate signal to a plurality of gate lines; and

a liquid crystal panel including the gate lines, the data lines and a plurality of switching elements disposed between the data lines and the gate lines;

wherein the timing controller comprises:

a data compensator to generate current frame first compensated grayscale data in response to receiving previous frame grayscale data from the memory and current frame grayscale data from an external source~~previously stored in the memory and grayscale data for a current frame;~~;

a grayscale modifier to generate current frame second compensated grayscale data in response to receiving the current frame first compensated grayscale data from the data compensator and a data difference between a previous frame second compensated grayscale data and a previous frame grayscale data, the data difference ~~the first compensated grayscale data and compensated grayscale data previously~~ stored in the memory; and

a difference calculator to calculate a data difference between the current frame second compensated grayscale data and the current frame grayscale data, the difference calculator receiving the current frame second compensated grayscale data from the grayscale modifier~~generate third compensated grayscale data in response to the grayscale data for a current frame and the second compensated grayscale data~~.

4. (Currently amended) The liquid crystal display apparatus according to claim 1, wherein the memory includes at least one frame memory for receiving and storing both the current frame grayscale data and the data difference between the current frame first compensated grayscale data and the current frame~~compensated~~ grayscale data.

5. (Currently amended) The liquid crystal display apparatus according to claim 4, wherein the frame memory stores the data difference between the current frame first compensated grayscale data and the current frame grayscale data, the data difference having a~~compensated grayscale data having the~~ number of bits substantially smaller than a~~the~~ number of bits of the current frame grayscale data.

6. (Original) The liquid crystal display apparatus according to claim 4, wherein the at least one frame memory includes a synchronous dynamic random access memory (SDRAM) or Double Date Rate (DDR) memory.

7. (Currently amended) The liquid crystal display apparatus according to claim 1, wherein the memory includes a first frame memory for receiving and storing current frame the grayscale data and a second frame memory for receiving and storing the data difference between the current frame first compensated grayscale data and the current frame ~~compensated~~ grayscale data.

8. (Original) The liquid crystal display apparatus according to claim 7, wherein the first and second frame memories each include a synchronous dynamic random access memory (SDRAM) or Double Date Rate (DDR) memory.

9. (Currently amended) The liquid crystal display apparatus according to claim 1 [[2]], wherein the data compensator includes a look-up table.

10. (Original) The liquid crystal display apparatus according to claim 3, wherein the data compensator includes a look-up table.

11. (Original) The liquid crystal display apparatus according to claim 1, wherein the liquid crystal panel includes a Patterned Vertical Alignment mode liquid crystal panel.

12. (Currently amended) The liquid crystal display apparatus according to claim 1 [[2]], wherein the current frame first compensated grayscale data includes overshoot data or undershoot data.

13. (Currently amended) The liquid crystal display apparatus according to claim 3, wherein the current frame first compensated grayscale data includes overshoot data or undershoot data.

14. (Currently amended) A method for driving a liquid crystal display apparatus, comprising:

generating current frame first compensated grayscale data in response to receiving previous frame grayscale data and current frame grayscale data received from an external source~~for a current frame and previously stored grayscale data for a previous frame~~;

calculating a data difference between the current frame first compensated grayscale data and the current frame grayscale data~~generating second compensated grayscale data in response to the first compensated grayscale data and the grayscale data for the current frame~~;

generating current frame second~~third~~ compensated grayscale data in response to the current frame first compensated grayscale data and the data difference between the previous frame compensated grayscale data and the previous frame grayscale data~~previously stored compensated grayscale data~~;

storing the current frame grayscale data ~~for the current frame~~ and the data difference in memory~~second compensated grayscale data~~;

applying a gate signal to gate lines; and

applying a data voltage corresponding to the current frame second~~third~~ compensated grayscale data to data lines.

15. (Currently amended) The method according to claim 14, wherein the current frame first compensated grayscale data includes overshoot data or undershoot data.

16. (Currently amended) The method according to claim 14, wherein storing includes storing the current frame grayscale data ~~for the current frame~~ and the data difference ~~second compensated grayscale data~~ in the same memory.

17. (Currently amended) The method according to claim 16, wherein the number of bits of the data difference ~~second compensated grayscale data~~ is less than the number of bits of the current frame grayscale data ~~for the current frame~~.

18. (Currently amended) The method according to claim 14, wherein storing includes storing the current frame grayscale data ~~for the current frame~~ in a first memory and storing the data difference~~second compensated grayscale data~~ in a second memory.

19. (Currently amended) A method for driving a liquid crystal display apparatus, comprising:

generating current frame first compensated grayscale data in response to receiving previous frame grayscale data and~~for a~~ current frame grayscale data received from an external source~~and previously stored grayscale data for a previous frame~~;

generating current frame second compensated grayscale data in response to receiving the current frame first compensated grayscale data and a data difference between a previous frame second compensated grayscale data and a previous frame grayscale data~~previously stored compensated grayscale data~~;

calculating a data difference between the current frame second compensated grayscale data and the current frame grayscale data~~generating third compensated grayscale data in response to the second compensated grayscale data for the current frame and the grayscale data for the current frame~~;

storing the current frame grayscale data and the data difference between the current frame second compensated grayscale data and the current frame grayscale data~~grayscale data and the third compensated grayscale data~~;

applying a gate signal to gate lines; and

applying a data voltage corresponding to the current frame second compensated grayscale data to data lines.

20. (Currently amended) The method according to claim 19, wherein the current frame first compensated grayscale data includes overshoot data or undershoot data.

21. (Currently amended) The method according to claim 19, wherein storing includes storing the current frame grayscale data ~~for the current frame~~ and the data difference between the current frame second compensated grayscale data and the current frame grayscale data~~third compensated grayscale data~~ in the same memory.

22. (Currently amended) The method according to claim 21, wherein the number of bits of the data difference between the current frame second compensated grayscale data and the current frame grayscale data~~third compensated grayscale data~~ is less than the number of bits of the current frame grayscale data ~~for the current frame~~.

23. (Currently amended) The method according to claim 19, wherein storing includes storing the current frame grayscale data ~~for the current frame~~ in a first memory and storing the data difference between the current frame second compensated grayscale data and the current frame grayscale ~~third compensated grayscale data~~ in a second memory.